Thunderhawk
TECHNOLOGY PARTNERS

INDUSTRY CAPABILITIES BRIEF

Semiconductors *& Advanced Manufacturing.*

The engineering muscle behind the silicon. Fab process, equipment, yield, and advanced-packaging talent for the US semiconductor build-out, calibrated to the cadence of fab ramp and the CHIPS-era expansion.

Fab Process Engineering | Equipment Engineering | Yield Engineering | Advanced Packaging | Design Verification & EDA | Fab Ramp & PM

Where we *go deep.*

Fab Process Engineering
FEOL, BEOL, litho, etch & CMP process engineers.

Equipment Engineering
ASML, AMAT, TEL / Lam, and KLA equipment engineers & tool-cal specialists.

Yield Engineering
Yield-ramp, defect-density, parametric, and SPC engineers.

Advanced Packaging
CoWoS, fan-out, 2.5D / 3D, and hybrid-bonding engineers.

Design Verification & EDA
RTL, UVM verification, Cadence & Synopsys specialists.

Fab Ramp-Up & Program Mgmt
Tool-qual, ramp, and multi-vendor program leads.

How clients *engage.*

Five engagement models: Contingent Workforce · SOW / Project Delivery · Managed Services (MSP & VMS) · Direct Hire · RPO

Built for the *CHIPS-era ramp.*

WBENC- & WOSB-certified (#WBE2600761 / #WOSB260585): a diverse-business partner with fab process, equipment, yield, and advanced-packaging depth for the domestic semiconductor build-out, delivered at the cadence of tool install, qual, and ramp.

Representative seats filled: etch / litho process engineers · process-integration & FEOL/BEOL specialists · equipment engineers (ASML / AMAT / KLA) · yield & defect-density engineers · CoWoS advanced-packaging engineers · UVM verification & RTL · fab-ramp managers.

Semiconductor *insights.*

AI & SOURCING	AI-augmented sourcing: separating real productivity from buzzword theater.	Read the insight →
CHIPS · TALENT	The clearance economy: how defense-tech entrants are repricing cleared talent.	Read the insight →
WORKFORCE STRATEGY	Time-to-fill in a tight market: what 30 days actually requires.	Read the insight →

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